(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 July 2002 (25.07.2002)

PCT

(10) International Publication Number
WO 02/058104 A1

(51) International Patent Classification[7]: H01J 40/14, H01L 27/146

(21) International Application Number: PCT/US01/50193

(22) International Filing Date: 19 October 2001 (19.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/696,919 26 October 2000 (26.10.2000) US

(71) Applicant: ROCKWELL SCIENTIFIC COMPANY LLC [US/US]; 1049 Camino Dos Rios, P.O. Box 1085, MCA15, Thousand Oaks, CA 91358-0085 (US).

(72) Inventor: KOZLOWSKI, Lester, J.; 212 Golden Fern Court, Simi Valley, CA 93065 (US).

(74) Agent: JOHNSON, Doyle, B.; Crosby, Heafey, Roach & May, Two Embarcadero Center, Suite 2000, San Francisco, CA 94111 (US).

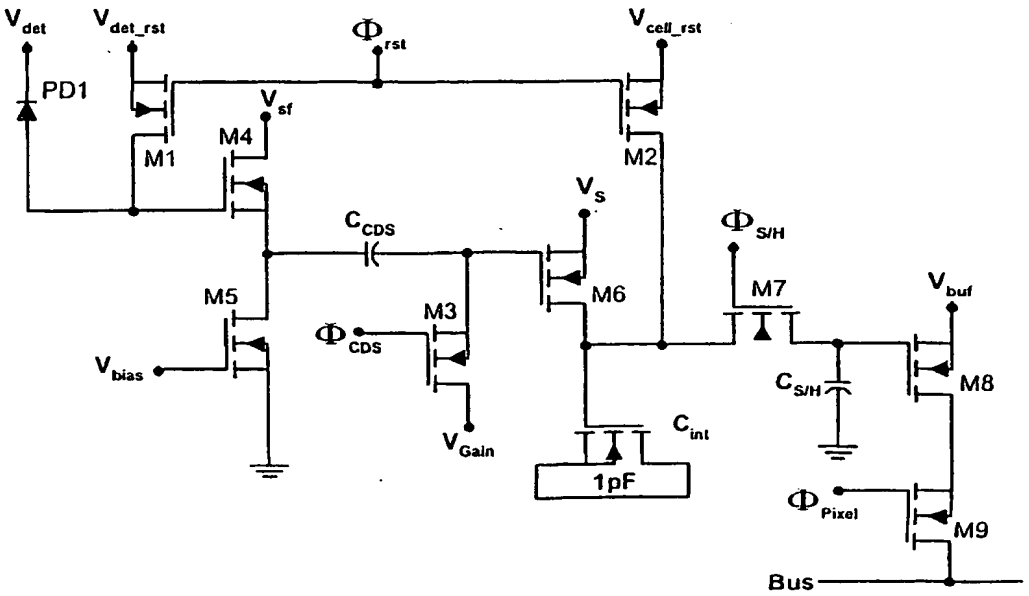
(81) Designated State *(national)*: JP.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: AMPLIFIED CMOS TRANSDUCER FOR SINGLE PHOTON READ-OUT OF PHOTODETECTORS



(57) Abstract: An ultra-low noise, high-gain interface pixel amplifier is provided with capability for single-photon readout of known photodetectors at high electrical bandwidths for diverse spectral bandpass from the x-ray to long IR bands. The detector charge (PD1) modulates a source follower (M4 and M5) whose output is double sampled to remove correlated noise by a compact stage that also facilitates low-noise gain adjustment for a second gain stage of programmable amplification. Single-photon readout of photodetectors at high electrical bandwidths in small pixel areas is thereby facilitated.

WO 02/058104 A1

AMPLIFIED CMOS TRANSDUCER FOR SINGLE PHOTON READ-OUT OF PHOTODETECTORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to photon detection, and more particularly to detector amplifiers for single photon read-out of semiconductor photodetectors in pixellated imaging arrays.

2. Description of the Related Art

Optical sensors transform incident radiant signals in the X - ray (λ<0.001μm), ultraviolet (λ=0.001 - 0.4μm), visible (λ=0.4 - 0.8μm), near infrared (IR) (λ=0.8 - 2μm), shortwave IR (λ=2.0 - 2.5μm), mid IR (λ=2.5 - 5μm), and long IR (λ=5 - 20μm) bands into electrical signals that are used for data collection, processing, storage and display, such as real-time video. Available conventional photodetectors such as photodiodes and photoconductors are inexpensive, exhibit bandwidths that support current video frame rates, are sensitive to wavelengths well into the long IR band, and exhibit a high degree of uniformity from pixel to pixel when used in an imaging array. However, these photodetectors have no gain, i.e. each incident photon generates, at most, a single electron. Thus, these imaging systems work well only in moderate to bright light conditions. At low light levels, they provide electrical signals that are too small to be read-out by conventional readout circuits.

In conditions of low ambient light, the standard photodetector is often replaced with an avalanche photodiode that provides significant gain such that conventional read-out circuits, such as charge coupled devices, i.e. CCDs, can read out the amplified signal at video frame rates with a high signal-to-noise ratio (SNR). The fabrication of avalanche photodiodes is much more difficult and expensive than standard photodetectors because they must simultaneously exhibit very high controlled gain and very low noise. Furthermore, currently available avalanche photodiodes exhibit relatively poor uniformity, are constrained to shorter wavelengths than standard photodetectors (0.7μm), and have limited sensitivity due to their relatively low quantum efficiency. Imaging intensified systems use an array of avalanche photodiodes or micro-channel

plates to drive respective display elements such as CCDs or phosphors, and have even lower wavelength capabilities (approximately 0.6μm max) due to the limitations of the photodiode.

Chamberlain et al. "A Novel Wide Dynamic Range Silicon photodetector and Linear Imaging Array" IEEE Transactions on Electron Devices, Vol. ED-31, No. 2, February 1984, pp. 175 - 182, herein incorporated by reference, describes a gate modulation technique for single photon read-out of standard photodetectors with wide dynamic range. Chamberlain provides a high-gain current mirror that includes a load FET (Field Effect Transistor) whose gate is connected to its drain to ensure sub-threshold operation. The signal from the photodetector is injected into the load FET thereby producing a signal voltage at the gate of a gain FET with high transconductance. This signal modulates the gain FET's gate voltage, which is read out and reset via a FET switch. The key benefit of this approach is that a detecting dynamic range of more than 10^7 for each detector in the array is produced. Unfortunately, the circuit is highly sensitive to variations in the threshold voltage of the various transistors. The pixel-to-pixel V_T non-uniformity associated with standard silicon CMOS fabrication processes degrades the instantaneous dynamic range of the imaging array even as the circuit's logarithmic characteristic enhances each pixel's ability to operate over a much larger total dynamic range.

Although this specific gain modulation technique is useful for detecting signals across a broad spectral range, the front-end bandwidth severely restricts the imaging array's bandwidth. Specifically, the dominant RC time constant is the parallel combination of the photodetector's capacitance and the resistance of the load FET. In sub-threshold operation, the FET's transconductance is very low and, hence, its load resistance is very large, at $\geq 10^{15}$ ohms; the minimum resulting RC time constant is on the order of tens of seconds. Chamberlain's gate modulation technique is thus only practically useful for imaging daylight scenes or static low-light-level scenes such as stars. Furthermore, to achieve large current gain, the load FET is typically quite small. As a result, the load FET exhibits substantial 1/f noise, which under low light conditions seriously degrades the performance of the imaging array.

U.S. Patent No. 5,933,190 discloses a circuit having a first reading transistor 23 in series with the load transistor of Chamberlain to read-out the voltage across the load transistor rather than the other leg of the current mirror. While this configuration self-biases the detectors in the imaging array, and the usable dynamic range for each pixel is still at least 10^7, the time constant is unchanged relative to Chamberlain's teaching. Further, the instantaneous dynamic range at a specific irradiance across an imaging array having pixels of such design is still highly sensitive to the threshold uniformity from transistor to transistor. The pixel-to-pixel V_T non-uniformity

BNSDOCID: <WO_02058104A1_I_>

associated with standard silicon CMOS fabrication processes degrades the instantaneous dynamic range of the imaging array even as the circuit's logarithmic characteristic enhances each pixel's ability to operate over a much larger total dynamic range. Though the '190 reference also teaches a method for reducing the non-uniformity by degrading the various transistors by applying a stressing over-voltage, this is definitely not a recommended procedure for a high-quality, long-life camera system.

U.S. Patent No. 5,929,434 teaches an alternative current mirror configuration that suppresses the impact of the V_T non-uniformity via an alternative current mirror configuration that also reads the integrated current after an integration period rather than the instantaneous voltage. The preferred embodiment minimizes, to first order, the variations in threshold non-uniformity by subtracting the non-uniformity within each pixel. Unfortunately, the residual pixel-to-pixel variations still dominate the imager's fixed pattern noise irrespective of background flux, depending on the MOS fabrication technology. The magnitude of pattern noise can often be larger than the signal, so off-chip compensation of pixel-to-pixel non-uniformity is required.

The negative feedback amplifier, A1, disclosed in U.S. Patent No. 5,929,434, significantly reduces the input impedance of the high-gain circuit and thereby enhances its bandwidth. In the case where the buffer amplifier is approximated to have infinite voltage gain and finite transconductance, the dominant pole is given by:

$$\tau_{B-L} = \frac{C_f}{g_{m_{Q1}}}$$

where C_f is the effective feedback capacitance of the buffer amplifier from its output to its input. Assuming a cascoded amplifier configuration, the gate-source capacitance of Q1 is dominant and C_f is set by the gate-to-source capacitance of the sub-threshold FET Q1. This is approximately given by the parasitic metal overlap capacitance. Assuming a minimum width transistor in 0.25μm CMOS technology, for example, the minimum C_f will be approximately 0.2 fF for transistors having minimum width. The resulting time constant is on the order of tenths of a second. Though this facilitates single photon sensing at roughly video frame rates, additional improvements are needed to truly support single-photon imaging at frame rates higher than typically used for standard video.

U.S. Patent No. 5,665,959 teaches yet another approach consisting of a digitized system wherein each pixel uses a pair of cascaded inverters with a sub-threshold transistor at its front-

BNSDOCID: <WO 02058104A1_I_>

end to generate extremely high transimpedance. Since the small photosignal at backgrounds on the order of one electron translates to extremely high input impedance, the photosignal is effectively integrated onto the Miller capacitance of a first-stage inverter prior to being further amplified by a second stage inverter. A resulting charge-to-voltage conversion gain >1 mV/e- is hence claimed. Nevertheless, the read noise of the charge-integrating first stage will limit the SNR for many practical cases since insufficient means are provided to band-limit the first amplifier's wideband noise. The read noise for the first stage can be approximated as similar to that of a charge integrator such that:

$$N_{stage_1} = \frac{1}{q}\sqrt{kTC_{fb}\cdot\frac{C_{\det}+C_{fb}}{C_L+\frac{C_{fb}\cdot C_{\det}}{C_{fb}+C_{\det}}}}$$

where k is Boltzmann's constant, T is the temperature, C_{fb} is the parasitic feedback capacitance of the first stage, C_{det} is the photodiode capacitance and C_L is the load capacitance at the amplifier's output. Assuming practical values consistent with the understanding of those skilled in the art, the detector capacitance is typically a minimum of 15 fF for the hybrid imager of the 5,665,959 preferred embodiment. Assuming a Miller capacitance for the first stage amplifier of 5 fF and a load capacitance of 350 fF (i.e., the storage capacitance C_{str1}), then the minimum read noise for the first stage will be in the range of 6 to 7 e-; this is on top of the kT/C noise generated by opening transistor switch Q_{SW1} to perform the offset compensation of the composite two-stage amplifier. This performance is very good, but does not facilitate photon counting. Further, while the clocking of the two-stage amplifier facilitates large reductions in amplifier non-uniformity, this invention does not suppress the threshold variations of the load resistor at the front end.

U.S. Patent No. 6,069,376 teaches a pixel amplifier with a speed switch suitable for still camera applications. This apparatus provides high-bandwidth signal integration with downstream gain, but its sensitivity is limited by the generation of reset noise at the storage element. Also, no facility is provided for maximizing the signal's dynamic range at the input to the amplifier.

BNSDOCID: <WO__02058104A1_I_>

SUMMARY OF THE INVENTION

In general, the present invention is a photodetector readout circuit, with extremely high sensitivity, capable of single-photon detection. A photodetector (preferably a photodiode) integrates a small-signal photocharge on the detector capacitance in response to incident photons, producing a photodetector output signal. A buffer amplifier is arranged to receive the photodetector output signal and to produce a buffered photodetector output signal. A coupling capacitor has a first terminal connected to the buffered output signal and a second terminal connected to a signal input of a signal amplifier. The coupling capacitor shifts a signal level at the input to the signal amplifier by an adjustable offset voltage. An electronic offset reset switch, connected to the coupling capacitor, allows resetting of the offset voltage, preferably just after reset of the photodiode to allow transient decay. The offset voltage is the reset noise (kTC) generated by resetting the detector capacitance.

To synchronize the start of image formation across a pixellated array, the reset is simultaneous across the entire array. Each pixel's offset voltage is clamped across each pixel's coupling capacitor by reading the specific detector's voltage, while simultaneously clamping the coupling capacitor to a specified voltage. When sampling of the photodiode signal begins, the actual signal is read relative to the offset voltage stored across the coupling capacitor. This effects correlated double sampling of the photogenerated signal, and eliminates the correlated noise generated by resetting (discharging) the photodetector capacitance. The clamping voltage is an adjustable voltage that also sets the quiescent operating point of the video signal amplifier above the threshold voltage of an integrating gain stage having common gate configuration and noise bandwidth set by a reset integrator.

The common gate amplifier provides large, adjustable current gain to further amplify the low-noise signal and integrate the boosted signal in a dedicated integration capacitor. At the end of a specified integration time, the integrated signal is sampled onto a second capacitor to synchronize the end of signal integration. Snapshot image capture is thus provided with very low noise referred back to the photodetector. The invention thereby improves transimpedance and dynamic range relative to prior solutions.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

RNSDOCID: <WO__02058104A1_I_>

Figure 1 is a schematic diagram of a generalized pixel amplifier in accordance with the present invention; and

Figure 2 is a schematic diagram of an alternative embodiment of the present invention in which the pixel amplifier enhances the instantaneous dynamic range and minimizes amplifier nonuniformity in exchange for lower transimpedance.

DETAILED DESCRIPTION OF THE INVENTION

The following description is provided to enable any person skilled in the art to make and use the invention and sets forth the best modes contemplated by the inventor for carrying out the invention. Various modifications, however, will remain readily apparent to those skilled in the art, since the basic principles of the present invention have been defined herein specifically to detector amplifier circuits for single photon read-out of semiconductor photodetectors in pixellated imaging arrays. Any and all such modifications, equivalents and alternatives are intended to fall within the spirit and scope of the present invention.

The present invention provides a high bandwidth, ultra low-noise pixel amplifier that is capable of single photon read-out of photodetectors in extremely low-light conditions, i.e. photon flux levels approaching zero photons per sampling period. This circuit can be used to effectively count incident photons on individual photodetectors, either in an imaging array as the front-end to a conventional video system or in high frame-rate wavefront sensors. One of the primary benefits of the approach is that the circuit can use off-the-shelf photodetectors such as photodiodes or photoconductors that have gain ≤ 1 rather than, for example, avalanche multiplication within the photodiode. Such known photodetectors with gain ≤ 1 are cheaper, more uniform, easier to fabricate, more reliable, less susceptible to excess noise mechanisms within the detector, and support a much broader range of the electromagnetic spectrum than avalanche photodiodes.

The generalized circuit in accordance with the present invention is shown in Figure 1. Before photodetection begins, enabling switch transistors M1 and M2 initializes the circuit to synchronize the subsequent start of signal integration across the pixellated array. In this initial state, any photo-generated charge on C_{pd} (which represents the capacitance of photodiode PD1) is discharged (reset) and the detector voltage is set to $V_{det} - V_{det_rst}$. Further, the signal integration capacitor, C_{int}, is set to V_{cell_rst}. Transistors M1 and M2 are subsequently disabled to allow the associated voltage transients to decay. Switch transistor M3 is then enabled to clamp C_{CDS} to V_{Gain}. This process stores each pixel's reset noise across C_{CDS} and sets the starting quiescent

BNSDOCID: <WO_02058104A1_I_>

voltage for the front-end amplifier. The front-end amplifier comprises a source follower buffer amplifier formed by transistors M4 and M5, the correlated double sampling capacitor C_{CDS}, and a switch transistor M3. By subsequently disabling switch transistor M3, the video signal established by the difference between the buffered photodetector signal and the clamped offset voltage subsequently modulates the gate of gain transistor M6. Transistor M6 is a common gate amplifier that supplies an adjustable current to integration transistor C_{int}. This current is adjusted by setting the difference between V_{Gain}-V_S and the threshold voltage of M5 since the source of M5 (V_S) is preferably operated at, or near, 0V to minimize pickup of bias-induced noise from the source terminal of M5. V_S is thus preferably set at ground for basic operation.

The current integrated in C_{int} is therefore a gain-proportioned facsimile of the photo-generated signal originally applied to source follower amplifier transistor M4. At the end of the prescribed integration time, switch transistor M7 is briefly enabled to store the signal voltage on the sample-and-hold capacitor $C_{S/H}$. This signal voltage modulates the gate of a second source follower amplifier transistor M8. The final signal voltage is read on a row-by-row basis to produce the video signal by enabling the switch transistor M9 via the Φ_{pixel} clock. The current sink for transistor M8 is typically common to all the pixels in each column and shared in this manner to minimize the power dissipation and the demand on support circuitry.

The output of the source follower transistor M4 is capacitively coupled by a series capacitor C_{CDS} initially, under control of a reset signal Φ_{CDS} applied to the gate of M3 at the start of integration. The clamping and sampling facilitated in this manner effects correlated double sampling of the photogenerated signal. This signal is essentially free of circuit-induced noise except for the 1/f noise of transistor M3. The correlated noise generated by resetting the detector capacitance is thereby eliminated. By minimizing the capacitances of PD1 and the gate of transistor M4, the basic transimpedance can be maximized to first order to minimize the required size of the capacitor C_{CDS}. To facilitate sub-electron read noise, the value of C_{CDS} must, at a minimum, be at least several femtofarads for operation at room temperature (295K).

The clamping circuit comprising the capacitor C_{CDS} and switch transistor M3, also effects a compact method for arbitrarily setting the minimum signal level at a quiescent operating point for compatibility with exercising either a portion of the available dynamic range, or the full dynamic range of the common gate amplifier. The clamping circuit thus provides both correlated double sampling and dynamic range management when the source terminal of transistor M6 is either connected to an externally accessible pad to enable external adjustment or biased by an adjustable on-chip reference voltage.

BNSDOCID: <WO 02058104A1_I_>

Since the transimpedance established by the combined capacitance of the detector and amplifier transistor M4 does not facilitate reading noise levels <10 e- at typical video rates, the present invention uses the level-shifting stage in conjunction with the common gate amplifier to effect large overall transimpedance. For example, the combined total capacitance of the photodetector and the gate of MOSFET M4 will practically be, at a minimum, ≥5 fF. The maximum photoconversion gain defined at the input to the compact amplifier is thus 32μV/e-. Because the minimum read noise referred to the output needs to be from 250μV to >1 mV in practical video cameras, the ability to detect quanta requires additional gain of from 10 to 30, at a minimum. Optimally adjusting the gate-to-source voltage by appropriately adjusting V_{GAIN} provides this additional gain. The output of the low-noise pixel amplifier is read from the pixel by enabling Φ_{pixel} to supply the signal to the bus via the switch transistor M9.

Figure 2 is a schematic circuit diagram of an alternative embodiment wherein the instantaneous dynamic range is increased from a maximum of about 10 bits to larger values depending on effective resistance of a switched-capacitor resistor placed at the source of common gate transistor M10. The programmable switched-capacitor resistor comprises transistor M10 and capacitor C_{dr} and reduces the gain of common gate amplifier M6 by adding a series resistance to the supply V_S. This source resistance increases the dynamic range and reduces the impact of the threshold voltage nonuniformity of transistor M10 in the pixellated array in exchange for lower overall transimpedance and adjustability. Alternatively, a high value fixed-resistor (0.5 to 50 MΩ) can replace transistor M10 and capacitor C_{dr} if a specific dynamic range or amplifier transimpedance is needed. The required value for the effective series resistance is that it acts as a current source. In order to do this, it must have a higher impedance than transistor M10. Looking into its source terminal, the resistance of transistor M10 is given by:

$$R_{M10} = \frac{1}{g_m + g_d}$$

where g_m is the FET transconductance and g_d is the drain conductance. In weak inversion or subthreshold operation, the resistance is thus g_m^{-1}; the resistance is g_d^{-1} in the linear region.

The ultra-low noise amplifiers of the present invention thus provide a total transimpedance that is approximately:

BNSDOCID: <WO 02058104A1 I >

$$Z_{T,Amp} = \frac{t_{\text{int}}}{C_{\text{det}} + C_{input}} \cdot \frac{q\Delta V_{sig}}{nkT} \cdot \frac{C_{\text{int}}}{C_{\text{det}} + C_{input}} \cdot A_{atten}$$

where t_{int} is the integration time, C_{int} is the integration capacitance, C_{det} is the detector capacitance, C_{input} is the combined capacitance of the source follower transistor and any other capacitances at this node, both stray and intentional, q is the electron charge, ΔV_{sig} is the integrated signal voltage programmed by tuning V_{gain} - V_s, n is the subthreshold ideality of transistor M6, k is Boltzmann's constant, T is the temperature, and A_{atten} is the attenuation facilitated by the series resistor. For the preferred embodiment, A_{atten}=1. The compact amplifier's gain is thus adjustable to compensate for transimpedance degradations resulting from either short integration time or large detector capacitance. The amplifier's gain can also be very large since ΔV_{sig} can be much larger than the thermal voltage of transistor M10 and capacitor C_{int} is often 10X to 100X larger than the sum (C_{det}+C_{input}). Nevertheless, for those sensors having large detector capacitance the former can still effect gains exceeding 100X.

The attenuation factor in the preceding equation is defined:

$$A_{atten} = \frac{R_{M10}}{R_{M10} + R_{SCR}}$$

where R_{SCR} is the effective resistance of the switched-capacitor resistor of the alternative embodiment. The preferred embodiment thus has no attenuation, i.e., A_{atten}=1 and the alternative embodiment can have attenuations from 1 to greater than 100.

Those skilled in the art will appreciate that various adaptations and modifications of the just-described preferred embodiments can be configured without departing from the scope and spirit of the invention. Therefore, it is to be understood that, within the scope of the appended claims, the invention may be practiced other than as specifically described herein.

ENSDOCID: <WO 02058104A1 | >

WHAT IS CLAIMED IS:

1. A single-photon read-out circuit, comprising:

a photodetector producing a photodetector output signal;

a buffer amplifier, arranged to receive the photodetector output signal, having a buffered photodetector output signal;

a signal amplifier having a signal input and a signal output;

a coupling capacitor, having a first terminal connected to the buffered output signal and a second terminal connected to the signal input of the signal amplifier; and

an electronic offset reset switch, connected to the coupling capacitor.

2. The circuit of Claim 1, further comprising a synchronization circuit connected to an input of the buffer amplifier and to the signal output of the signal amplifier.

3. The circuit of Claim 2, further comprising an integration capacitor connected to the signal output of the signal amplifier.

4. The circuit of Claim 3, further comprising a sample-and-hold circuit connected to the signal output of the signal amplifier.

5. The circuit of Claim 4, further comprising an output amplifier connected to the sample-and-hold circuit.

6. The circuit of Claim 5, further comprising a variable current source connected to the signal amplifier.

7. The circuit of Claim 6, wherein the buffer amplifier comprises two MOSFETs arranged in a source follower configuration.

8. The circuit of Claim 7, wherein the signal amplifier comprises a MOSFET.

9. The circuit of Claim 8, wherein the offset reset switch comprises a MOSFET.

BNSDOCID: <WO 02058104A1_I_>

10. The circuit of Claim 9, wherein the synchronization circuit comprises two MOSFETs having a reset signal connected to each gate.

11. The circuit of Claim 10, wherein the sample-and-hold circuit comprises a MOSFET and a capacitor.

12. The circuit of Claim 11, wherein the variable current source comprises a MOSFET and a capacitor.

13. A single-photon read-out circuit, comprising:

a photodetector that integrates a small-signal photocharge on a detector capacitance in response to incident photons, producing a photodetector output signal;

a buffer amplifier, arranged to receive the photodetector output signal and to produce a buffered photodetector output signal;

a signal amplifier having a signal input and producing a signal output;

a coupling capacitor, having a first terminal connected to the buffered output signal and a second terminal connected to the signal input of the signal amplifier, to shift a signal level by an offset voltage; and

an electronic offset reset switch, connected to the coupling capacitor, for resetting the offset voltage.

14. The circuit of Claim 13, further comprising a synchronization circuit connected to an input of the buffer amplifier and to the output signal of the signal amplifier to synchronize a start of signal integration across a pixellated array.

15. The circuit of Claim 14, further comprising a sample-and-hold circuit for storing a signal voltage.

16. The circuit of Claim 15, further comprising a variable current source for connected to the signal amplifier for increasing an instantaneous dynamic range of the circuit.

BNSDOCID: <WO 02058104A1 I >

17. A signal read-out circuit comprising:

a photodetector connected to a detector voltage;

a first MOSFET having a gate connected to the photodetector, and a drain connected to a first voltage;

a second MOSFET having a drain connected to a source of the first MOSFET, and a gate connected to a first bias voltage;

a correlated double sampling capacitor having a first terminal connected to the source of the first MOSFET;

a signal amplifier MOSFET having a gate connected to a second terminal of the correlated double sampling capacitor, and a source connected to a second voltage;

an electronic offset reset switch MOSFET having a source connected to the second terminal of the correlated double sampling capacitor, a drain connected to a gain voltage, and a gate connected to a correlated double sampling signal; and

an integration capacitor connected to the drain of the signal amplifier MOSFET.

18. The circuit of Claim 17, further comprising:

a sample-and-hold MOSFET having a source connected to the drain of the signal amplifier MOSFET, and a gate connected to a sample-and-hold signal; and

a sample-and-hold capacitor connected to a drain of the sample-and-hold MOSFET.

19. The circuit of Claim 18, further comprising:

a first reset MOSFET having a drain connected to the gate of the first MOSFET, a gate connected to a reset signal, and a source connected to a detector reset voltage; and

a second reset MOSFET having a drain connected to the drain of the signal amplifier, a gate connected to the reset signal, and a source connected to a cell reset voltage.

20. The circuit of Claim 19, further comprising:

an amplifier MOSFET having a source connected to a buffer voltage, a gate connected to the drain of the sample-and-hold MOSFET; and

an access MOSFET having a source connected to a drain of the amplifier MOSFET, a gate connected to an access signal, and a drain connected to a bus.

BNSDOCID: <WO__02058104A1_I_>

21. The circuit of Claim 17, further comprising:

a dynamic range MOSFET having a drain connected to the source of the signal amplifier MOSFET, a source connected to a source voltage, and a gate connected to a dynamic range signal; and

a dynamic range capacitor connected to the drain of the dynamic range MOSFET.

BNSDOCID: <WO__02058104A1_I_>

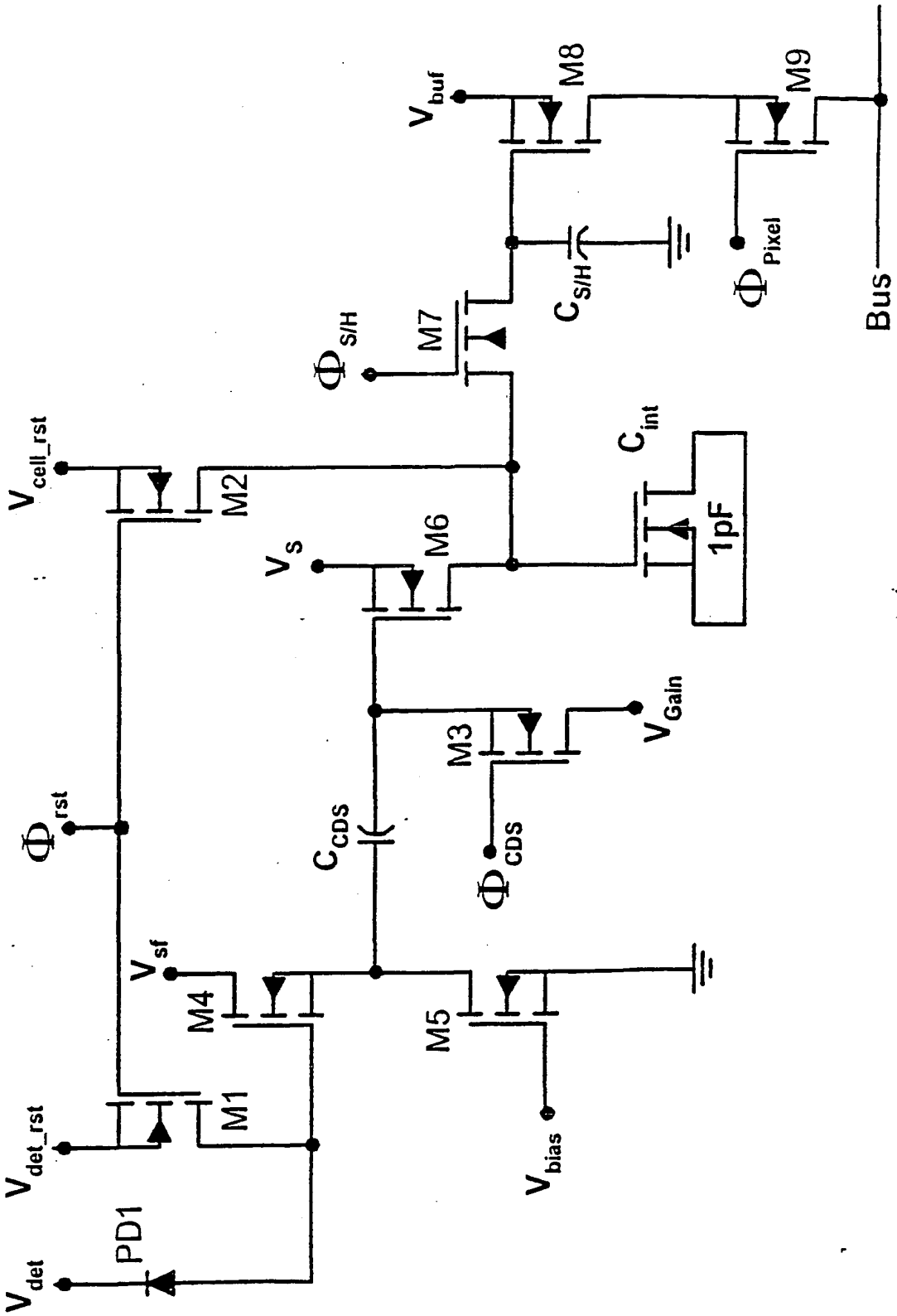


FIGURE 1

BNSDOCID: <WO__02058104A1_I_>

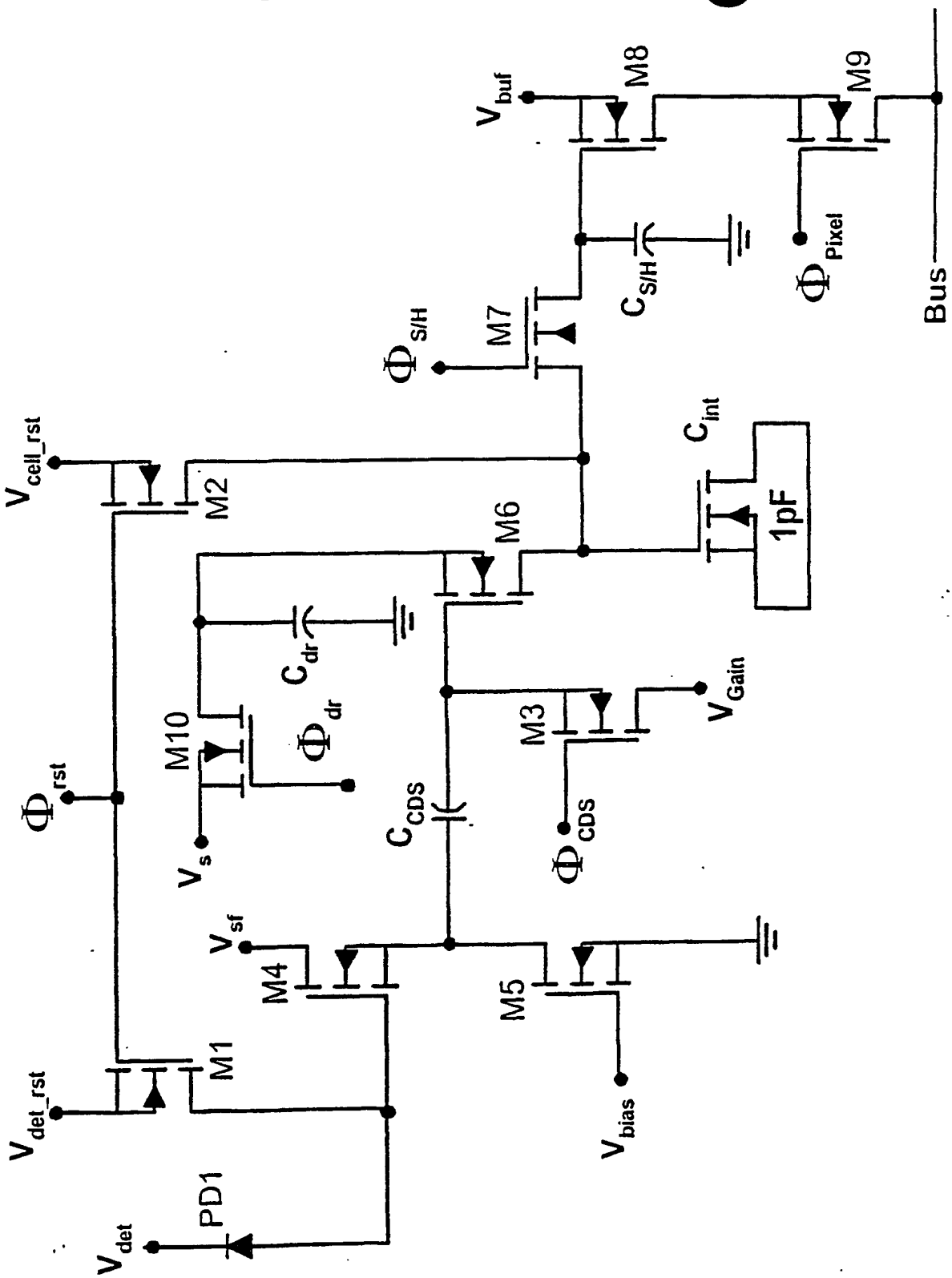


FIGURE 2

BNSDOCID: <WO__02058104A1_I_>

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/50193

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01J 40/14; H01L 27/146
US CL : 250/214A, 208.1; 348/294

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 250/214A, 208.1, 214LA, 214R; 348/294, 297, 300, 301, 308; 330/59; 257/290-292; 377/60

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST
Search terms:(((correlated adj double adj sampling) or cds), buffer adj amplifier$2.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,892,540 A (KOZLOWSKI et al.) 06 April 1999 (06.04.1999), see entire document	1, 13, 17
X	US 5,233,180 A (TSURUTA et al.) 03 August 1993 (03.08.1993), see entire document.	1, 13, 17
X	US 5,280,511 A (FUJII et al.) 18 January 1994 (18.01.1994), See entire document.	1, 13, 17
---		---
Y		21
Y	US 5,929,434 A (KOZLOWSKI et al.) 27 July 1999 (27.07.1999), See entire document.	21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 May 2002 (09.05.2002)	27 JUN 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer SEUNG C. SOHN Telephone No. (703) 308-4093

Form PCT/ISA/210 (second sheet) (July 1998)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

CORRECTED VERSION

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 July 2002 (25.07.2002)

PCT

(10) International Publication Number
WO 02/058104 A1

(51) International Patent Classification[7]: H01J 40/14, H01L 27/146

(21) International Application Number: PCT/US01/50193

(22) International Filing Date: 19 October 2001 (19.10.2001)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/696,919 26 October 2000 (26.10.2000) US

(71) Applicant: ROCKWELL SCIENTIFIC COMPANY LLC [US/US]; 1049 Camino Dos Rios, P.O. Box 1085, MCA15, Thousand Oaks, CA 91358-0085 (US).

(72) Inventor: KOZLOWSKI, Lester, J.; 212 Golden Fern Court, Simi Valley, CA 93065 (US).

(74) Agent: JOHNSON, Doyle, B.; Crosby, Heafey, Roach & May, Two Embarcadero Center, Suite 2000, San Francisco, CA 94111 (US).

(81) Designated State *(national)*: JP.

(84) Designated States *(regional)*: European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

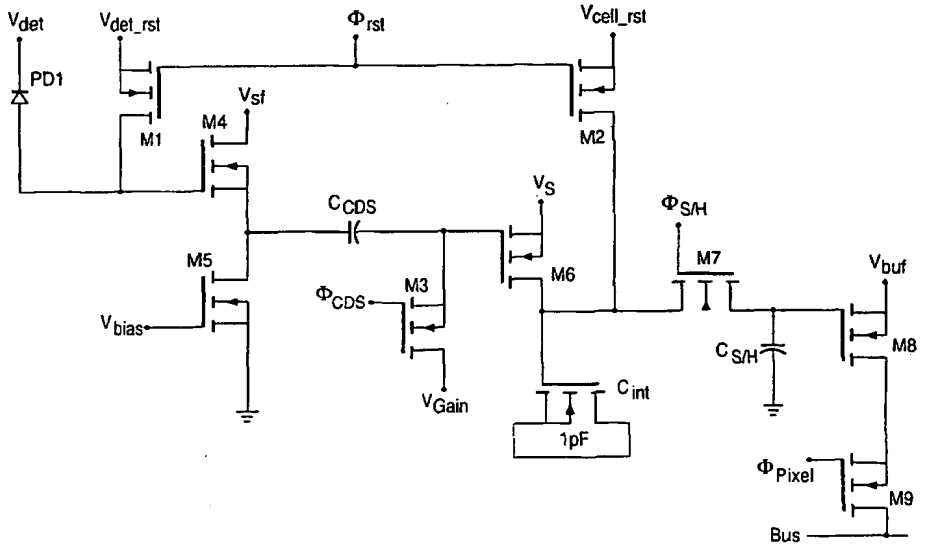
Published:
— *with international search report*

(48) Date of publication of this corrected version:
14 August 2003

(15) Information about Correction:
see PCT Gazette No. 33/2003 of 14 August 2003, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: AMPLIFIED CMOS TRANSDUCER FOR SINGLE PHOTON READ-OUT OF PHOTODETECTORS



(57) Abstract: An ultra-low noise, high-gain interface pixel amplifier is provided with capability for single-photon readout of known photodetectors at high electrical bandwidths for diverse spectral bandpass from the x-ray to long IR bands. The detector charge (PD1) modulates a source follower (M4 and M5) whose output is double sampled to remove correlated noise by a compact stage that also facilitates low-noise gain adjustment for a second gain stage of programmable amplification. Single-photon readout of photodetectors at high electrical bandwidths in small pixel areas is thereby facilitated.

WO 02/058104 A1

BNSDOCID: <WO_ 02058104A1_IA>

AMPLIFIED CMOS TRANSDUCER FOR SINGLE PHOTON READ-OUT OF PHOTODETECTORS

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to photon detection, and more particularly to detector amplifiers for single photon read-out of semiconductor photodetectors in pixellated imaging arrays.

2. Description of the Related Art

Optical sensors transform incident radiant signals in the X - ray (λ<0.001μm), ultraviolet (λ=0.001 - 0.4μm), visible (λ=0.4 - 0.8μm), near infrared (IR) (λ=0.8 - 2μm), shortwave IR (λ=2.0 - 2.5μm), mid IR (λ=2.5 - 5μm), and long IR (λ=5 - 20μm) bands into electrical signals that are used for data collection, processing, storage and display, such as real-time video. Available conventional photodetectors such as photodiodes and photoconductors are inexpensive, exhibit bandwidths that support current video frame rates, are sensitive to wavelengths well into the long IR band, and exhibit a high degree of uniformity from pixel to pixel when used in an imaging array. However, these photodetectors have no gain, i.e. each incident photon generates, at most, a single electron. Thus, these imaging systems work well only in moderate to bright light conditions. At low light levels, they provide electrical signals that are too small to be read-out by conventional readout circuits.

In conditions of low ambient light, the standard photodetector is often replaced with an avalanche photodiode that provides significant gain such that conventional read-out circuits, such as charge coupled devices, i.e. CCDs, can read out the amplified signal at video frame rates with a high signal-to-noise ratio (SNR). The fabrication of avalanche photodiodes is much more difficult and expensive than standard photodetectors because they must simultaneously exhibit very high controlled gain and very low noise. Furthermore, currently available avalanche photodiodes exhibit relatively poor uniformity, are constrained to shorter wavelengths than standard photodetectors (0.7μm), and have limited sensitivity due to their relatively low quantum efficiency. Imaging intensified systems use an array of avalanche photodiodes or micro-channel

BNSDOCID: <WO 02058104A1 IA>

plates to drive respective display elements such as CCDs or phosphors, and have even lower wavelength capabilities (approximately 0.6μm max) due to the limitations of the photodiode.

Chamberlain et al. "A Novel Wide Dynamic Range Silicon photodetector and Linear Imaging Array" IEEE Transactions on Electron Devices, Vol. ED-31, No. 2, February 1984, pp. 175 - 182, herein incorporated by reference, describes a gate modulation technique for single photon read-out of standard photodetectors with wide dynamic range. Chamberlain provides a high-gain current mirror that includes a load FET (Field Effect Transistor) whose gate is connected to its drain to ensure sub-threshold operation. The signal from the photodetector is injected into the load FET thereby producing a signal voltage at the gate of a gain FET with high transconductance. This signal modulates the gain FET's gate voltage, which is read out and reset via a FET switch. The key benefit of this approach is that a detecting dynamic range of more than 10^7 for each detector in the array is produced. Unfortunately, the circuit is highly sensitive to variations in the threshold voltage of the various transistors. The pixel-to-pixel V_T non-uniformity associated with standard silicon CMOS fabrication processes degrades the instantaneous dynamic range of the imaging array even as the circuit's logarithmic characteristic enhances each pixel's ability to operate over a much larger total dynamic range.

Although this specific gain modulation technique is useful for detecting signals across a broad spectral range, the front-end bandwidth severely restricts the imaging array's bandwidth. Specifically, the dominant RC time constant is the parallel combination of the photodetector's capacitance and the resistance of the load FET. In sub-threshold operation, the FET's transconductance is very low and, hence, its load resistance is very large, at $\geq 10^{15}$ ohms; the minimum resulting RC time constant is on the order of tens of seconds. Chamberlain's gate modulation technique is thus only practically useful for imaging daylight scenes or static low-light-level scenes such as stars. Furthermore, to achieve large current gain, the load FET is typically quite small. As a result, the load FET exhibits substantial 1/f noise, which under low light conditions seriously degrades the performance of the imaging array.

U.S. Patent No. 5,933,190 discloses a circuit having a first reading transistor 23 in series with the load transistor of Chamberlain to read-out the voltage across the load transistor rather than the other leg of the current mirror. While this configuration self-biases the detectors in the imaging array, and the usable dynamic range for each pixel is still at least 10^7, the time constant is unchanged relative to Chamberlain's teaching. Further, the instantaneous dynamic range at a specific irradiance across an imaging array having pixels of such design is still highly sensitive to the threshold uniformity from transistor to transistor. The pixel-to-pixel V_T non-uniformity

BNSDOCID: <WO_02058104A1_IA>

associated with standard silicon CMOS fabrication processes degrades the instantaneous dynamic range of the imaging array even as the circuit's logarithmic characteristic enhances each pixel's ability to operate over a much larger total dynamic range. Though the '190 reference also teaches a method for reducing the non-uniformity by degrading the various transistors by applying a stressing over-voltage, this is definitely not a recommended procedure for a high-quality, long-life camera system.

U.S. Patent No. 5,929,434 teaches an alternative current mirror configuration that suppresses the impact of the V_T non-uniformity via an alternative current mirror configuration that also reads the integrated current after an integration period rather than the instantaneous voltage. The preferred embodiment minimizes, to first order, the variations in threshold non-uniformity by subtracting the non-uniformity within each pixel. Unfortunately, the residual pixel-to-pixel variations still dominate the imager's fixed pattern noise irrespective of background flux, depending on the MOS fabrication technology. The magnitude of pattern noise can often be larger than the signal, so off-chip compensation of pixel-to-pixel non-uniformity is required.

The negative feedback amplifier, A1, disclosed in U.S. Patent No. 5,929,434, significantly reduces the input impedance of the high-gain circuit and thereby enhances its bandwidth. In the case where the buffer amplifier is approximated to have infinite voltage gain and finite transconductance, the dominant pole is given by:

$$\tau_{B-L} = \frac{C_f}{g_{m_{Q1}}}$$

where C_f is the effective feedback capacitance of the buffer amplifier from its output to its input. Assuming a cascoded amplifier configuration, the gate-source capacitance of Q1 is dominant and C_f is set by the gate-to-source capacitance of the sub-threshold FET Q1. This is approximately given by the parasitic metal overlap capacitance. Assuming a minimum width transistor in 0.25μm CMOS technology, for example, the minimum C_f will be approximately 0.2 fF for transistors having minimum width. The resulting time constant is on the order of tenths of a second. Though this facilitates single photon sensing at roughly video frame rates, additional improvements are needed to truly support single-photon imaging at frame rates higher than typically used for standard video.

U.S. Patent No. 5,665,959 teaches yet another approach consisting of a digitized system wherein each pixel uses a pair of cascaded inverters with a sub-threshold transistor at its front-

BNSDOCID: <WO 02058104A1 IA>

end to generate extremely high transimpedance. Since the small photosignal at backgrounds on the order of one electron translates to extremely high input impedance, the photosignal is effectively integrated onto the Miller capacitance of a first-stage inverter prior to being further amplified by a second stage inverter. A resulting charge-to-voltage conversion gain >1 mV/e- is hence claimed. Nevertheless, the read noise of the charge-integrating first stage will limit the SNR for many practical cases since insufficient means are provided to band-limit the first amplifier's wideband noise. The read noise for the first stage can be approximated as similar to that of a charge integrator such that:

$$N_{stage_1} = \frac{1}{q}\sqrt{kTC_{fb}\cdot\frac{C_{\det}+C_{fb}}{C_L+\frac{C_{fb}\cdot C_{\det}}{C_{fb}+C_{\det}}}}$$

where k is Boltzmann's constant, T is the temperature, C_{fb} is the parasitic feedback capacitance of the first stage, C_{det} is the photodiode capacitance and C_L is the load capacitance at the amplifier's output. Assuming practical values consistent with the understanding of those skilled in the art, the detector capacitance is typically a minimum of 15 fF for the hybrid imager of the 5,665,959 preferred embodiment. Assuming a Miller capacitance for the first stage amplifier of 5 fF and a load capacitance of 350 fF (i.e., the storage capacitance C_{stor1}), then the minimum read noise for the first stage will be in the range of 6 to 7 e-; this is on top of the kT/C noise generated by opening transistor switch Q_{SW1} to perform the offset compensation of the composite two-stage amplifier. This performance is very good, but does not facilitate photon counting. Further, while the clocking of the two-stage amplifier facilitates large reductions in amplifier non-uniformity, this invention does not suppress the threshold variations of the load resistor at the front end.

U.S. Patent No. 6,069,376 teaches a pixel amplifier with a speed switch suitable for still camera applications. This apparatus provides high-bandwidth signal integration with downstream gain, but its sensitivity is limited by the generation of reset noise at the storage element. Also, no facility is provided for maximizing the signal's dynamic range at the input to the amplifier.

BNSDOCID: <WO_02058104A1_IA>

SUMMARY OF THE INVENTION

In general, the present invention is a photodetector readout circuit, with extremely high sensitivity, capable of single-photon detection. A photodetector (preferably a photodiode) integrates a small-signal photocharge on the detector capacitance in response to incident photons, producing a photodetector output signal. A buffer amplifier is arranged to receive the photodetector output signal and to produce a buffered photodetector output signal. A coupling capacitor has a first terminal connected to the buffered output signal and a second terminal connected to a signal input of a signal amplifier. The coupling capacitor shifts a signal level at the input to the signal amplifier by an adjustable offset voltage. An electronic offset reset switch, connected to the coupling capacitor, allows resetting of the offset voltage, preferably just after reset of the photodiode to allow transient decay. The offset voltage is the reset noise (kTC) generated by resetting the detector capacitance.

To synchronize the start of image formation across a pixellated array, the reset is simultaneous across the entire array. Each pixel's offset voltage is clamped across each pixel's coupling capacitor by reading the specific detector's voltage, while simultaneously clamping the coupling capacitor to a specified voltage. When sampling of the photodiode signal begins, the actual signal is read relative to the offset voltage stored across the coupling capacitor. This effects correlated double sampling of the photogenerated signal, and eliminates the correlated noise generated by resetting (discharging) the photodetector capacitance. The clamping voltage is an adjustable voltage that also sets the quiescent operating point of the video signal amplifier above the threshold voltage of an integrating gain stage having common gate configuration and noise bandwidth set by a reset integrator.

The common gate amplifier provides large, adjustable current gain to further amplify the low-noise signal and integrate the boosted signal in a dedicated integration capacitor. At the end of a specified integration time, the integrated signal is sampled onto a second capacitor to synchronize the end of signal integration. Snapshot image capture is thus provided with very low noise referred back to the photodetector. The invention thereby improves transimpedance and dynamic range relative to prior solutions.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be readily understood by the following detailed description in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and in which:

BNSDOCID: <WO _02058104A1_IA>

Figure 1 is a schematic diagram of a generalized pixel amplifier in accordance with the present invention; and

Figure 2 is a schematic diagram of an alternative embodiment of the present invention in which the pixel amplifier enhances the instantaneous dynamic range and minimizes amplifier nonuniformity in exchange for lower transimpedance.

DETAILED DESCRIPTION OF THE INVENTION

The following description is provided to enable any person skilled in the art to make and use the invention and sets forth the best modes contemplated by the inventor for carrying out the invention. Various modifications, however, will remain readily apparent to those skilled in the art, since the basic principles of the present invention have been defined herein specifically to detector amplifier circuits for single photon read-out of semiconductor photodetectors in pixellated imaging arrays. Any and all such modifications, equivalents and alternatives are intended to fall within the spirit and scope of the present invention.

The present invention provides a high bandwidth, ultra low-noise pixel amplifier that is capable of single photon read-out of photodetectors in extremely low-light conditions, i.e. photon flux levels approaching zero photons per sampling period. This circuit can be used to effectively count incident photons on individual photodetectors, either in an imaging array as the front-end to a conventional video system or in high frame-rate wavefront sensors. One of the primary benefits of the approach is that the circuit can use off-the-shelf photodetectors such as photodiodes or photoconductors that have gain ≤ 1 rather than, for example, avalanche multiplication within the photodiode. Such known photodetectors with gain ≤ 1 are cheaper, more uniform, easier to fabricate, more reliable, less susceptible to excess noise mechanisms within the detector, and support a much broader range of the electromagnetic spectrum than avalanche photodiodes.

The generalized circuit in accordance with the present invention is shown in Figure 1. Before photodetection begins, enabling switch transistors M1 and M2 initializes the circuit to synchronize the subsequent start of signal integration across the pixellated array. In this initial state, any photo-generated charge on C_{pd} (which represents the capacitance of photodiode PD1) is discharged (reset) and the detector voltage is set to $V_{det} - V_{det_rst}$. Further, the signal integration capacitor, C_{int}, is set to V_{cell_rst}. Transistors M1 and M2 are subsequently disabled to allow the associated voltage transients to decay. Switch transistor M3 is then enabled to clamp C_{CDS} to V_{Gain}. This process stores each pixel's reset noise across C_{CDS} and sets the starting quiescent

BNSDOCID: <WO_02058104A1_IA>

voltage for the front-end amplifier. The front-end amplifier comprises a source follower buffer amplifier formed by transistors M4 and M5, the correlated double sampling capacitor C_{CDS}, and a switch transistor M3. By subsequently disabling switch transistor M3, the video signal established by the difference between the buffered photodetector signal and the clamped offset voltage subsequently modulates the gate of gain transistor M6. Transistor M6 is a common gate amplifier that supplies an adjustable current to integration transistor C_{int}. This current is adjusted by setting the difference between V_{Gain}-V_S and the threshold voltage of M5 since the source of M5 (V_S) is preferably operated at, or near, 0V to minimize pickup of bias-induced noise from the source terminal of M5. V_S is thus preferably set at ground for basic operation.

The current integrated in C_{int} is therefore a gain-proportioned facsimile of the photo-generated signal originally applied to source follower amplifier transistor M4. At the end of the prescribed integration time, switch transistor M7 is briefly enabled to store the signal voltage on the sample-and-hold capacitor $C_{S/H}$. This signal voltage modulates the gate of a second source follower amplifier transistor M8. The final signal voltage is read on a row-by-row basis to produce the video signal by enabling the switch transistor M9 via the Φ_{pixel} clock. The current sink for transistor M8 is typically common to all the pixels in each column and shared in this manner to minimize the power dissipation and the demand on support circuitry.

The output of the source follower transistor M4 is capacitively coupled by a series capacitor C_{CDS} initially, under control of a reset signal Φ_{CDS} applied to the gate of M3 at the start of integration. The clamping and sampling facilitated in this manner effects correlated double sampling of the photogenerated signal. This signal is essentially free of circuit-induced noise except for the 1/f noise of transistor M3. The correlated noise generated by resetting the detector capacitance is thereby eliminated. By minimizing the capacitances of PD1 and the gate of transistor M4, the basic transimpedance can be maximized to first order to minimize the required size of the capacitor C_{CDS}. To facilitate sub-electron read noise, the value of C_{CDS} must, at a minimum, be at least several femtofarads for operation at room temperature (295K).

The clamping circuit comprising the capacitor C_{CDS} and switch transistor M3, also effects a compact method for arbitrarily setting the minimum signal level at a quiescent operating point for compatibility with exercising either a portion of the available dynamic range, or the full dynamic range of the common gate amplifier. The clamping circuit thus provides both correlated double sampling and dynamic range management when the source terminal of transistor M6 is either connected to an externally accessible pad to enable external adjustment or biased by an adjustable on-chip reference voltage.

BNSDOCID: <WO 02058104A1_IA>

Since the transimpedance established by the combined capacitance of the detector and amplifier transistor M4 does not facilitate reading noise levels <10 e- at typical video rates, the present invention uses the level-shifting stage in conjunction with the common gate amplifier to effect large overall transimpedance. For example, the combined total capacitance of the photodetector and the gate of MOSFET M4 will practically be, at a minimum, ≥5 fF. The maximum photoconversion gain defined at the input to the compact amplifier is thus 32μV/e-. Because the minimum read noise referred to the output needs to be from 250μV to >1 mV in practical video cameras, the ability to detect quanta requires additional gain of from 10 to 30, at a minimum. Optimally adjusting the gate-to-source voltage by appropriately adjusting V_{GAIN} provides this additional gain. The output of the low-noise pixel amplifier is read from the pixel by enabling Φ_{pixel} to supply the signal to the bus via the switch transistor M9.

Figure 2 is a schematic circuit diagram of an alternative embodiment wherein the instantaneous dynamic range is increased from a maximum of about 10 bits to larger values depending on effective resistance of a switched-capacitor resistor placed at the source of common gate transistor M10. The programmable switched-capacitor resistor comprises transistor M10 and capacitor C_{dr} and reduces the gain of common gate amplifier M6 by adding a series resistance to the supply V_S. This source resistance increases the dynamic range and reduces the impact of the threshold voltage nonuniformity of transistor M10 in the pixellated array in exchange for lower overall transimpedance and adjustability. Alternatively, a high value fixed-resistor (0.5 to 50 MΩ) can replace transistor M10 and capacitor C_{dr} if a specific dynamic range or amplifier transimpedance is needed. The required value for the effective series resistance is that it acts as a current source. In order to do this, it must have a higher impedance than transistor M10. Looking into its source terminal, the resistance of transistor M10 is given by:

$$R_{M10} = \frac{1}{g_m + g_d}$$

where g_m is the FET transconductance and g_d is the drain conductance. In weak inversion or subthreshold operation, the resistance is thus g_m^{-1}; the resistance is g_d^{-1} in the linear region.

The ultra-low noise amplifiers of the present invention thus provide a total transimpedance that is approximately:

BNSDOCID: <WO_02058104A1_IA>

$$Z_{T,Amp} = \frac{t_{\text{int}}}{C_{\text{det}} + C_{input}} \cdot \frac{q\Delta V_{sig}}{nkT} \cdot \frac{C_{\text{int}}}{C_{\text{det}} + C_{input}} \cdot A_{atten}$$

where t_{int} is the integration time, C_{int} is the integration capacitance, C_{det} is the detector capacitance, C_{input} is the combined capacitance of the source follower transistor and any other capacitances at this node, both stray and intentional, q is the electron charge, ΔV_{sig} is the integrated signal voltage programmed by tuning V_{gain} - V_s, n is the subthreshold ideality of transistor M6, k is Boltzmann's constant, T is the temperature, and A_{atten} is the attenuation facilitated by the series resistor. For the preferred embodiment, A_{atten}=1. The compact amplifier's gain is thus adjustable to compensate for transimpedance degradations resulting from either short integration time or large detector capacitance. The amplifier's gain can also be very large since ΔV_{sig} can be much larger than the thermal voltage of transistor M10 and capacitor C_{int} is often 10X to 100X larger than the sum (C_{det}+C_{input}). Nevertheless, for those sensors having large detector capacitance the former can still effect gains exceeding 100X.

The attenuation factor in the preceding equation is defined:

$$A_{atten} = \frac{R_{M10}}{R_{M10} + R_{SCR}}$$

where R_{SCR} is the effective resistance of the switched-capacitor resistor of the alternative embodiment. The preferred embodiment thus has no attenuation, i.e., A_{atten}=1 and the alternative embodiment can have attenuations from 1 to greater than 100.

Those skilled in the art will appreciate that various adaptations and modifications of the just-described preferred embodiments can be configured without departing from the scope and spirit of the invention. Therefore, it is to be understood that, within the scope of the appended claims, the invention may be practiced other than as specifically described herein.

BNSDOCID: <WO 02058104A1 IA>

WHAT IS CLAIMED IS:

1. A single-photon read-out circuit, comprising:

a photodetector producing a photodetector output signal;

a buffer amplifier, arranged to receive the photodetector output signal, having a buffered photodetector output signal;

a signal amplifier having a signal input and a signal output;

a coupling capacitor, having a first terminal connected to the buffered output signal and a second terminal connected to the signal input of the signal amplifier; and

an electronic offset reset switch, connected to the coupling capacitor.

2. The circuit of Claim 1, further comprising a synchronization circuit connected to an input of the buffer amplifier and to the signal output of the signal amplifier.

3. The circuit of Claim 2, further comprising an integration capacitor connected to the signal output of the signal amplifier.

4. The circuit of Claim 3, further comprising a sample-and-hold circuit connected to the signal output of the signal amplifier.

5. The circuit of Claim 4, further comprising an output amplifier connected to the sample-and-hold circuit.

6. The circuit of Claim 5, further comprising a variable current source connected to the signal amplifier.

7. The circuit of Claim 6, wherein the buffer amplifier comprises two MOSFETs arranged in a source follower configuration.

8. The circuit of Claim 7, wherein the signal amplifier comprises a MOSFET.

9. The circuit of Claim 8, wherein the offset reset switch comprises a MOSFET.

BNSDOCID: <WO__02058104A1_IA>

10. The circuit of Claim 9, wherein the synchronization circuit comprises two MOSFETs having a reset signal connected to each gate.

11. The circuit of Claim 10, wherein the sample-and-hold circuit comprises a MOSFET and a capacitor.

12. The circuit of Claim 11, wherein the variable current source comprises a MOSFET and a capacitor.

13. A single-photon read-out circuit, comprising:

a photodetector that integrates a small-signal photocharge on a detector capacitance in response to incident photons, producing a photodetector output signal;

a buffer amplifier, arranged to receive the photodetector output signal and to produce a buffered photodetector output signal;

a signal amplifier having a signal input and producing a signal output;

a coupling capacitor, having a first terminal connected to the buffered output signal and a second terminal connected to the signal input of the signal amplifier, to shift a signal level by an offset voltage; and

an electronic offset reset switch, connected to the coupling capacitor, for resetting the offset voltage.

14. The circuit of Claim 13, further comprising a synchronization circuit connected to an input of the buffer amplifier and to the output signal of the signal amplifier to synchronize a start of signal integration across a pixellated array.

15. The circuit of Claim 14, further comprising a sample-and-hold circuit for storing a signal voltage.

16. The circuit of Claim 15, further comprising a variable current source for connected to the signal amplifier for increasing an instantaneous dynamic range of the circuit.

BNSDOCID: <WO_02058104A1_IA>

17. A signal read-out circuit comprising:

a photodetector connected to a detector voltage;

a first MOSFET having a gate connected to the photodetector, and a drain connected to a first voltage;

a second MOSFET having a drain connected to a source of the first MOSFET, and a gate connected to a first bias voltage;

a correlated double sampling capacitor having a first terminal connected to the source of the first MOSFET;

a signal amplifier MOSFET having a gate connected to a second terminal of the correlated double sampling capacitor, and a source connected to a second voltage;

an electronic offset reset switch MOSFET having a source connected to the second terminal of the correlated double sampling capacitor, a drain connected to a gain voltage, and a gate connected to a correlated double sampling signal; and

an integration capacitor connected to the drain of the signal amplifier MOSFET.

18. The circuit of Claim 17, further comprising:

a sample-and-hold MOSFET having a source connected to the drain of the signal amplifier MOSFET, and a gate connected to a sample-and-hold signal; and

a sample-and-hold capacitor connected to a drain of the sample-and-hold MOSFET.

19. The circuit of Claim 18, further comprising:

a first reset MOSFET having a drain connected to the gate of the first MOSFET, a gate connected to a reset signal, and a source connected to a detector reset voltage; and

a second reset MOSFET having a drain connected to the drain of the signal amplifier, a gate connected to the reset signal, and a source connected to a cell reset voltage.

20. The circuit of Claim 19, further comprising:

an amplifier MOSFET having a source connected to a buffer voltage, a gate connected to the drain of the sample-and-hold MOSFET; and

an access MOSFET having a source connected to a drain of the amplifier MOSFET, a gate connected to an access signal, and a drain connected to a bus.

BNSDOCID: <WO__02058104A1_IA>

21. The circuit of Claim 17, further comprising:

a dynamic range MOSFET having a drain connected to the source of the signal amplifier MOSFET, a source connected to a source voltage, and a gate connected to a dynamic range signal; and

a dynamic range capacitor connected to the drain of the dynamic range MOSFET.

BNSDOCID: <WO 02058104A1 IA>

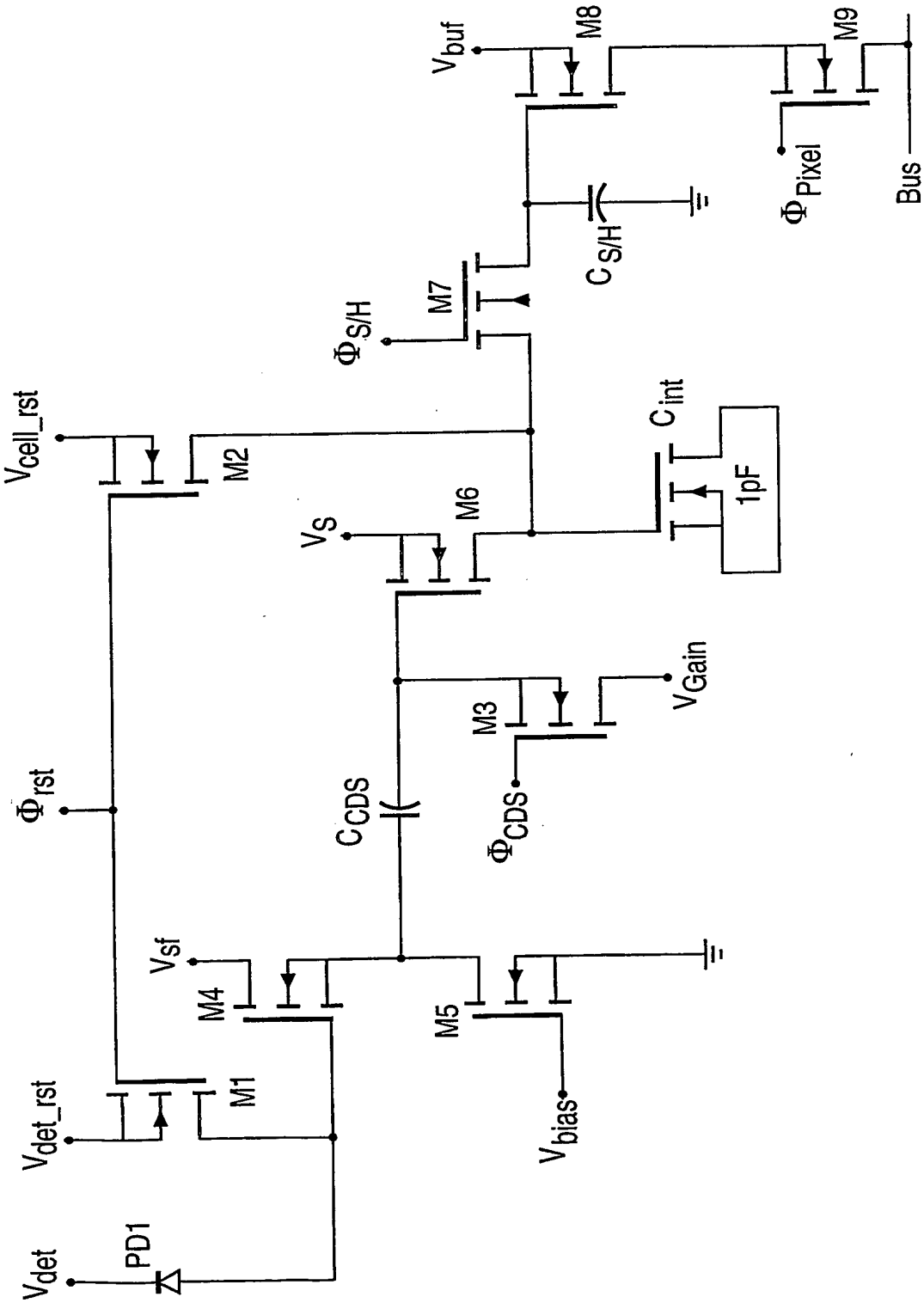


FIGURE 1

BNSDOCID: <WO__02058104A1_IA>

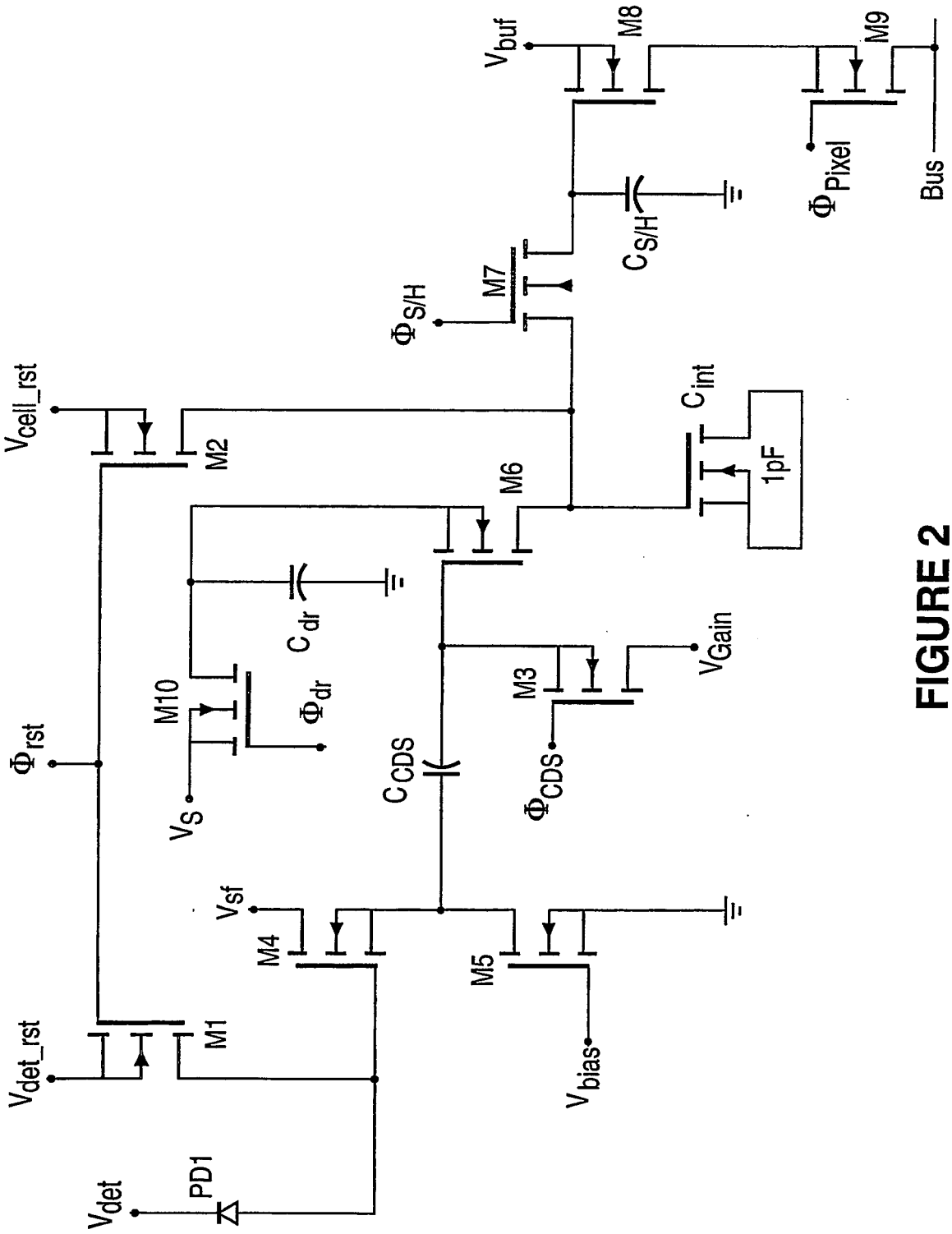


FIGURE 2

BNSDOCID: <WO__02058104A1_IA>

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US01/50193

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H01J 40/14; H01L 27/146
US CL : 250/214A, 208.1; 348/294

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 250/214A, 208.1, 214LA, 214R; 348/294, 297, 300, 301, 308; 330/59; 257/290-292; 377/60

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EAST
Search terms:(((correlated adj double adj sampling) or cds), buffer adj amplifier$2.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,892,540 A (KOZLOWSKI et al.) 06 April 1999 (06.04.1999), see entire document	1, 13, 17
X	US 5,233,180 A (TSURUTA et al.) 03 August 1993 (03.08.1993), see entire document.	1, 13, 17
X	US 5,280,511 A (FUJII et al.) 18 January 1994 (18.01.1994), See entire document.	1, 13, 17
Y		21
Y	US 5,929,434 A (KOZLOWSKI et al.) 27 July 1999 (27.07.1999), See entire document.	21

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 May 2002 (09.05.2002)	27 JUN 2002
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer SEUNG C. SOHN Telephone No. (703) 308-4093

Form PCT/ISA/210 (second sheet) (July 1998)

BNSDOCID: <WO_02058104A1_IA>

THIS PAGE BLANK (USPTO)